A modified Shichman-Hodges model for OTFTs usable in the Quite Universal Circuit Simulator

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***Abstract*— Emergent transistor technologies are based on nanomaterials, which may improve device performance and may lead to novel electronic applications. Whereas circuit models for silicon technologies are highly advanced, device modeling for emergent technologies faces huge challenges like ever-changing material processing and device architectures. Therefore, the development time for compact transistor models have to be reduced. The present case study analyses measured DC current-voltage curves of a top-gate top-contact (TGTC) organic thin film transistor (OTFT) to illustrate the capacity of the Quite Universal Circuit Simulator (QUCS) as an efficient platform for developing transistor models based on emerging technologies. First, model parameters for two established models were extracted namely for the Shichman-Hodges (SH) FET model and for the Unified Model and Extraction Method (UMEM). Second, a smoothing function known from JFET models has been applied to the SH model, combining the linear and saturation regions of the transistor in a single equation. The modified Shichman-Hodges (mSH) model was successfully implemented in QUCS as equation-defined device (EDD) and as Verilog-A code. The mSH model improved the fitting of the measured electrical characteristics of the selected TGTC OTFT.**

***Index Terms*—Circuit simulation, Nanoelectronics, Organic thin film transistors, Open source software, Semiconductor device modeling**

I. Introduction

MATERIAL innovation for electronic devices focus today on nanomaterials like pure carbon, zinc oxide, black phosphorous or conductive organic molecules. New materials require often new electron device architectures and compact models are not readily available. However, computer aided design and simulation of benchmark circuits is a powerful tool to estimate the expected performance that a given transistor technology platform can deliver. The demand for calibrated and predictive circuit models for novel transistor technologies may be even higher than for established contenders since theoretical performance projections help to attract venture capital necessary to fully develop the corresponding processing platform.

Organic electronics is a rapidly growing technological field employing the semiconducting properties of small molecules or polymers for realizing lightweight electronics through solution-based manufacturing techniques. Although research on organic electronics has been pursued for a longer period, interest sparked in the 1980s when the performance of organic devices increased significantly [1]. Today organic devices target application areas not easily covered by silicone devices. Organic field-effect transistors (OFETs) are representative devices that form a basic building block for various microelectronic systems. Compact models for OFETs gain importance as the demand moves from device-level investigation towards circuit-level integration. OFETs are normally realized as thin-film devices with the electrical contacts at the bottom or the top of the active layer (top-gate top-contact, top-gate bottom-contact, bottom-gate top-contact or bottom-gate bottom-contact OTFTs), depending on the application and its demands. The development of compact transistor models has in recent years profited significantly from the use of equation-defined non-linear functional elements and the use of Verilog-A as the preferred hardware description language for model construction and model interchange between different circuit simulators, primarily because of its extensive modeling capabilities and ease of use [2].

The Quite Universal Circuit Simulator (QUCS) is an open source circuit simulator developed by a group of international scientists and engineers under the GNU General Public License (GPL) [3], [4]. QUCSs release 0.0.11 introduced equation-defined devices (EDD) as a modeling tool allowing to create tailored descriptions of new devices and subroutines [5]. Release 0.0.12 enabled Verilog-A modeling, which has become the standard for device models since it creates high-level behavioral and structural descriptions, encapsulated in easily readable codes [6]. Since the adoption by the QUCS circuit simulation community, EDD and Verilog-A modules of compact device models became an attractive option for nonlinear device model development for emerging technologies.

In this paper, we present the implementation of a modified Shichman-Hodges model as equation-defined device and Verilog-A code in QUCS. Moreover, we implemented the Unified Model and parameter Extraction Method (UMEM) [7] in the available circuit simulation platform for the purpose to

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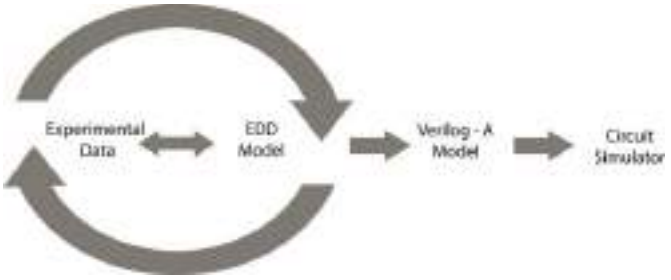

Fig. 1. Suggested implementation path showing the chronological order of device model development for emergent transistor technologies.

benchmark the mSH model. UMEM uses analytical expressions for both modeling and parameter extraction, so calculations can be performed using any program for mathematical computations. The main advantage of this method is that all above threshold parameters are extracted from two transfer characteristics, one in the linear and the other in the saturation region, and from the output characteristic of the device under study, using a single mathematical algorithm based on an integral method that additionally reduces experimental noise. The method can be used to compare devices with different geometries and fabrication conditions under the same parameter extraction conditions. We implemented the extraction algorithm in the numerical computing environment MATLAB.

II. Methodology

In QUCS, an EDD model is a non-linear component with up to eight branches, and this limit may be increased, if necessary [5]. Algebraic functions of a great number of variables such as voltage, current, admittance and so on can be implemented in a very similar to C-coding environment. Therefore, the user can consider particularities of the device behavior just by creating equations to define or refine the actuation of the corresponding model [8]. A stable EDD model allows interactive development of new non-linear components and a Verilog-A coding helps in the deployment and distribution of the newly developed models. Although EDD models are slow, they are very useful in de-bugging and can be easily translated afterwards into a hardware description language. The principal development and deployment flux is illustrated in Fig. 1. Due to the highly interactive model improvement, it must be expected that development time is greatly reduced compared to traditional schemes. QUCS inherently supports this strategy. Verilog-A codes are implemented in QUCS using an ADMS compiler and a XML interface [2].

The well-known SH model [9] uses a controlled current source to describe the drain current (I_D) as follows [10]:

$$I_D = \beta_p \times \begin{cases} 0; & |V_{GS}| \le |V_{th}| \\ (V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}; & |V_{DS}| \le |V_{GS}| - |V_{th}| \\ \frac{(V_{GS} - V_{th})^2}{2}; & |V_{DS}| \ge |V_{GS}| - |V_{th}| \end{cases}$$

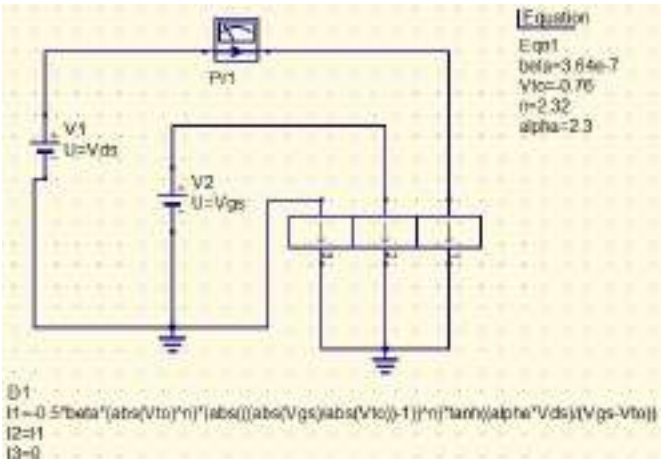

Fig. 2. Schematic for the implemented EDD mSH model.

The pre-factor β_p can be determined from a technology parameter K_P and a geometry factor W/L but is here used as model parameter. The SH model describes the three operational regions of the FET, cut-off, linear and saturation, by three distinct equations. The mSH model combines the linear and saturation regions into a single equation giving a smoother transition compared to the original model, which predicts a more abrupt switch-over. The modified equation describes the current using basically the same parameters, but with the elegant adding of a hyperbolic tangent, as follows:

$$I_D = \frac{\beta_k}{2}|V_{th}|^n\left(\frac{V_{GS}}{V_{th}} - 1\right)^n \tanh\left(\frac{\alpha V_{DS}}{V_{GS} - V_{th}}\right)$$

The model parameters of the mSH model are V_{th}, β_k (which have similar meanings like their counterparts in the original SH model) n and α. The additional mathematical parameters n and α adjust the linear-to-saturation transition. For small V_{DS} the hyperbolic tangent turns into a linear function describing the linear operation region of the FET, the parameter α describing basically the inclination. For large arguments, *i.e.*, in the saturation region, the hyperbolic tangent approaches one and the only V_{DS} dependence stems from the channel modulation included in β_p as in the original SH model. A sub-threshold current is not included in the mSH model, *i.e.*, $I_D = 0$ for $|V_{GS}| \le |V_{th}|$. Even though the described smoothing function is well known in the literature, it should be noted that a corresponding model is not readily available in QUCS. Therefore, the given modification serves as an example of demonstrating the flexibility of QUCS in implementing new or modified models. Moreover, the mSH model is a useful addition to the model library for describing organic thin-film transistors for future researches and further implementation.

Following the suggested development strategy depicted in Fig. 1, the mSH model was first implemented directly as EDD. The schematic of the EDD based mSH model is shown in Fig. 2. The EDD mSH model is a three branches device. The user must insert one equation for current and for charge, for each of the three branches. The charge equations are assumed to be zero, since no charge-based model is used. Once each terminal

TABLE I
EXTRACTED PARAMETERS FOR THE SH, MSH AND UMEM MODEL. DUE TO HYSTERESIS EFFECTS, PARAMETER VALUES MAY BE EXTRACTED SEPARATELY FOR THE OUTPUT AND TRANSFER CURVES. THIS MAY LEAD TO VERY DIFFERENT PARAMETER SETS AS DEMONSTRATED HERE FOR THE MSH MODEL.

Model	Parameter	Value (Transfer)	Value (Output)	Unit
SH	V_{th}	-0.76	-0.76	V
	β_p	$6.02 \cdot 10^{-7}$	$6.02 \cdot 10^{-7}$	AV^{-2}
mSH	V_{th}	-0.365	-0.76	V
	β_k	$3.64 \cdot 10^{-7}$	$3.64 \cdot 10^{-7}$	AV^{-n}
	α	0.05	2.3	–
	n	4	2.32	–
UMEM	V_{th}	-1.19	-1.19	V
	γ	0.396	0.396	–
	α_s	0.66	0.66	–
	m	1.476	1.476	–
	λ	-0.02	-0.02	V^{-1}
	RS	$3.325 \cdot 10^3$	$3.325 \cdot 10^3$	Ω
	RD	$3.325 \cdot 10^3$	$3.325 \cdot 10^3$	Ω
	V_{aa}	24.142	24.142	V

has its equation, the model is ready to be used. We employed the EDD mSH model for parameter extraction from the experimental output and transfer curve of a TGTC OTFT. Parameter extraction proceeded in an iterative manner to encounter the best values fitting the experimental current-voltage curves.

Finally, after EDD implementation and verification of the usefulness of the model, the mSH model was subsequently implemented as Verilog-A code. The EDD version of the model serves as high-level model template, which allows also regression testing of the Verilog-A code. To this extend it must be verified that both methods return the same results. The successfully implemented and tested Verilog-A code can be easily deployed to different circuit simulators.

Aside from the in-house development of compact models for emergent transistor technologies, it is interesting to implement models described in the literature to compare and test their validity for a given characterized transistor. QUCS is an ideal platform since the implementation as EDD or Verilog-A code is readily available. We have implemented and tested several compact models, both for organic thin-film transistors, like UMEM and MVS [11], [12], and for carbon nanotube based technologies, like CCAM [13], [14]. Here we use our QUCS implementation of the UMEM model [7], [15], [16] to benchmark the quality of the developed mSH model.

III. RESULTS

Experimental transfer and output characteristics were provided by the Chair for Electron Devices and Integrated Circuits (CEDIC) hosted by the *Technische Universität Dresden* (TUD), Germany. An organic thin-film transistor with a channel length of $L = 50\mu m$ and a gate width of $W = 1000\mu m$ has been electrically characterized. Source and drain contacts as well as the gate contact were positioned at the top of the device (TGTC OTFT). As a starting point, we extracted the parameters of a standard SH FET model based on the provided experimental output and transfer characteristics. The

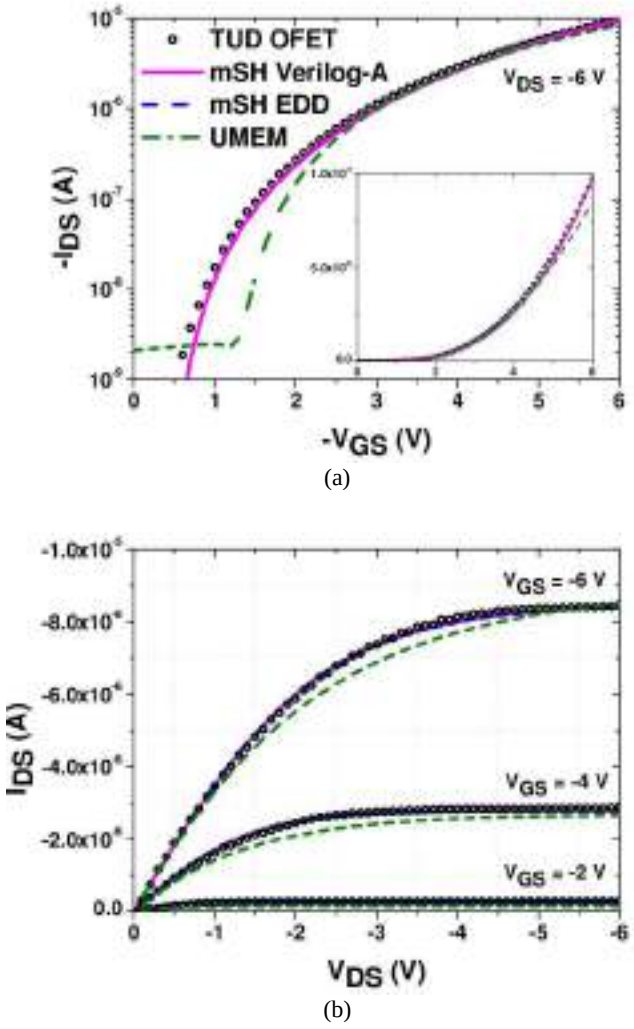

Fig. 3. Comparison of measured electrical characteristics of a TGTC OTFT with simulations employing the mSH and UMEM model: (a) Transfer curve for $V_{DS} = -6\,V$ on a semi-log scale and on a linear scale (inset); (b) Output curve for $V_{GS} = -6\,V, -4\,V$ and $-2\,V$. The legend of (a) applies also to (b).

determined parameter values are given in Table I. The fitting of the measured output and transfer curves proved to be rather poor.

As previously described, we extracted the model parameters of the mSH EDD and the UMEM model. The corresponding values are also given in Table I. UMEM parameter determination employed an automatic extraction algorithm implemented in MATLAB. On the contrary, parameters for the SH and mSH model were extracted manually. Although extraction algorithms have a great advantage in efficiency they rely on a sufficient amount of data points, which was not given in the present case study. Since contact resistance values are high in organic devices, a source R_S and drain R_D resistance is included in the UMEM model. Internal and external voltages are related via $V_{DS} = V'_{DS} + I_D(R_S + R_D)$ and $V_{GS} = V'_{GS} + I_D R_D$. Regarding the other UMEM parameters: α_S is a saturation parameter, m is an inflection parameter of the output characteristic, V_{th} is the

threshold voltage, V_{aa} is a low field mobility parameter, γ modifies the mobility dependence on $(V_{GS} - V_{th})$ and λ is the output conductance. Two sets of parameters are necessary to describe the transfer and output curve separately. The reason are hysteresis effects, common for emergent technologies, which lead to a different drain current for the same bias point depending on the sequence of ramping the voltages. We considered two different parameters sets only for the mSH model. Note that in a circuit simulator a unique parameter set has to be employed.

We compare the simulated output and transfer curves of the two models with the experimental data in Fig. 3. As can be seen, the mSH model describes the experimental findings very well. The surprisingly good agreement points to the fact that the investigated TGTC OTFT behaves like a nearly ideal long channel transistor. Interestingly, no serial resistances were required to explain the measured voltage dependence on the drain voltage whereas the UMEM algorithm extracted drain and source resistances of several $k\Omega$. Fig. 3 (a) includes also a comparison between the mSH EDD and Verilog-A model implementation. Such comparisons, *i.e.* regression testing, can be used to confirm that both implementations are equivalent. The simultaneous availability of both implementation methods in QUCS proves therefore to be very useful for transistor model development. Fig. 3 (a) demonstrates also that the extracted parameter set for the UMEM model gives some discrepancies at gate voltages below $|V_{GS}| < 2$ V. These discrepancies are due to the limited experimental data available to extract the parameters. UMEM is an advanced model for organic FETs and employs an automatic parameter extraction algorithm. However, the algorithm needs both linear and saturation transfer curves for successful parameter extraction, which often are not available. We used data inter- and extrapolation to increase the number of data points. However, this proved to be not sufficient. Moreover, the UMEM extraction algorithm delivers a unique set of model parameters, taking into account hysteresis shifts during extraction. For the mSH model we extracted manually and by purpose two very different parameters sets to illustrate the difficulties encountered by model development for emergent technologies, since a unique parameter set is a necessary pre-requisite for circuit simulations.

Fig. 4 shows the transconductance g_m as a function of the gate voltage derived from the transfer curve. Due to the sparse measurement points, there is considerable noise when calculating numerically the derivative of the drain current of the gate voltage. The mSH model predicts a gate voltage dependence of g_m, which reasonable well smoothens the experimental curve. Since the transconductance essentially determines the gain of amplifier stages, transistors are often biased to give a specified g_m value. Therefore, a good transistor model to be used in circuit simulations has to predict the transconductance correctly. The mSH model fulfills this requirement.

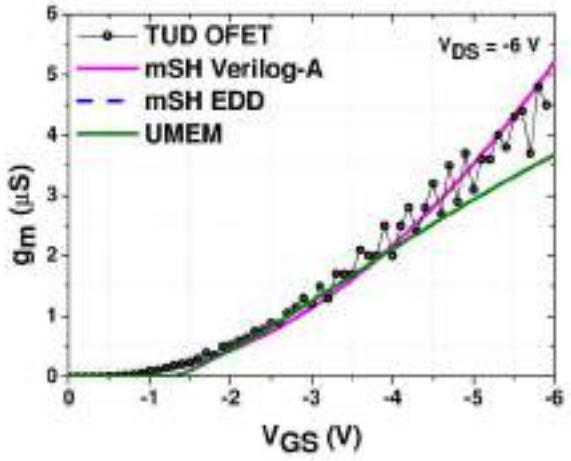

Fig. 4. Dependence of the transconductance g_m on the gate voltage. The mSH models smoothens the noisy experimental data very well.

IV. Conclusion

We extracted model parameters for the SH, mSH and UMEM model from DC characteristics of a top-gate top-contact organic thin-film transistor. The mSH model improved the linear-to-saturation crossover by substituting the square-law behavior of the SH model by a hyperbolic tangent, providing two additional parameters to adjust the low-bias channel conductance independent of the saturation behavior. Surprisingly, the mSH model described the measured DC current-voltage curves even better than the extracted UMEM model, an advanced model specifically developed for thin-film transistors.

The present case study demonstrates a new model development flow, implementing model equations first as equation-defined device, which allows fast interactive iterations to improve the current-voltage relation governing the electrical characteristics. Only after a satisfying set of equations is found, the model is implemented in a device description language like Verilog-A. The latter implementation can be easily deployed to different circuit simulators. Moreover, the EDD implementation can be used for regression testing of the Verilog-A code. Such a development flow should prove especially useful for emergent technologies. Since these technologies are still under development, there is a continuous demand of new transistor models.

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